**Lab 3**

**OBJECTIVES:**

* Max terms and Min terms
* To learn and study how to create and test combinational logic circuit on trainer
* To simplify Boolean expression and its usage to obtain cost effective circuit for implementation

**EQUIPMENT:** Logic trainer, Logic probe

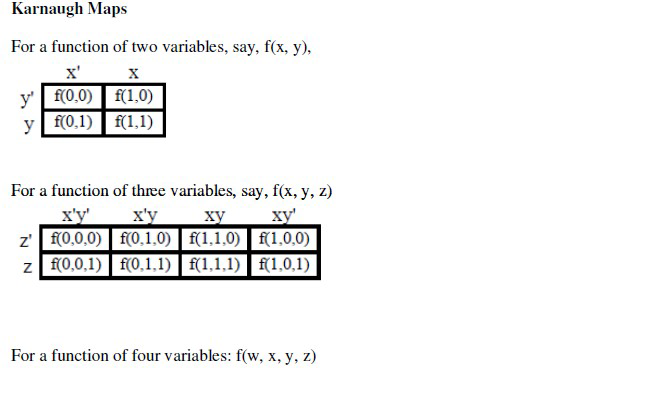
**COMPONENTS:** ICs 74LS08, 74LS32, 74LS04

**THEORY:**

When a Boolean expression is implemented with logic gates, each term requires a gate, and each variable within the term designates an input to the gate. We define a **literal** as a single variable within the term that may or may not be complemented. By reducing the number of terms, the number of literals, or both in a Boolean expression, it is often possible to reduce the cost of circuit and obtain a simpler circuit. **Boolean algebra is applied to reduce an expression for obtaining a simpler circuit.** A Boolean function can be written in a variety of ways when expressed algebraically. There are, however, a few ways of writing algebraic expressions that are considered to be standard forms. The standard forms facilitate the simplification procedures for Boolean expressions and frequently result in more desirable logic circuits.

The standard forms contain product terms and sum terms. An example of a product term is XYZ. This is a logical product consisting of an AND operation among three literals. An example of a sum term is X+Y+Z. This is a logical sum consisting of OR operation among the literals. Any Boolean expression can be written in form of **SOP and POS forms.**

A Boolean function can be represented by a **Karnaugh map** in which each cell corresponds to a minterm. The cells are arranged in such a way that any two immediately adjacent cells correspond to two minterms of distance 1. There is more than one way to construct a map with this property.



**Max terms and min terms:**

**Q1:**

**Find Max terms from the following Min terms**

1. F (X, Y,Z) =Σm(1,3,6,7)
2. F(X,Y,Z) =Σm(0,1,2,4,6)
3. F(A,B,C) =Σm(0,3,4,5,7)

**Q2:**

**For the Boolean function do the following:**

1. Find truth table
2. Find minimal SOP expression for Boolean function
3. Simply the F1 using Boolean Properties and Implement it on Hardware
4. Simply the F1 using Boolean Properties and Implement it on Hardware
5. Fill the following table for reduced using Boolean Properties

|  |  |  |  |
| --- | --- | --- | --- |
| IC type | Required No. of Gates | Gates per IC | Required No. of ICs |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
| Total no. of ICs | | |  |

1. Fill the following table for reduced using K-Maps

|  |  |  |  |
| --- | --- | --- | --- |
| IC type | Required No. of Gates | Gates per IC | Required No. of ICs |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
|  |  |  |  |
| Total no. of ICs | | |  |

**Q3. For the Boolean functions implement the circuit and make a truth table**

**F1 = A’C + AB’ + B (**using only AND and NOT gates)

**F2 = AB + A’C (**using only OR and NOT gates)